REMARKS

The following is intended as a full and complete response to the Final Office Action dated June 23, 2010, having a shortened statutory period for response set to expire on September 23, 2010. The Examiner rejected claims 1, 4-12 and 17-28 under 35 U.S.C. §103(a) as being unpatentable over Van Hook (U.S. Patent No. 6,342,892) in view of Suzuoki (U.S. Patent No. 6,526,491). The Examiner also rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over Van Hook in view of Suzuoki and Intel (Intel PCI and PCI Express).

Rejections under Double Patenting

The Examiner provisionally rejected claims 1, 4-12 and 16-28 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7, 10-17 and 25-40 of co-pending Application No. 10/715,459 and over claims 1, 5-19 and 26-35 of co-pending Application No. 10/839,155. Applicants acknowledge the double patenting rejection made in the Final Office Action and respectfully request that the rejection be held in abeyance until the pending claims are in condition for allowance. At such time, if still necessary, an appropriate terminal disclaimer will be filed.

Rejections under 35 U.S.C. § 103(a)

Claim 1, as previously presented, recites the limitations of a hardware-based physics processing unit (PPU) comprising a floating point engine (FPE) that includes a vector processor adapted to perform multiple, parallel floating point operations to generate physics data, the operations specified by a very long instruction word that is issued to the FPE, a PPU control engine (PCE) configured to control the overall operation of the PPU by allocating memory resources within an internal memory to the FPE and distributing commands received from a host central processing unit (CPU) to the FPE for processing, and a data movement engine (DME) configured to control the movement of data between the external memory and the internal memory in response to instructions received from the PCE. None of the cited references teaches or suggests these different limitations.

Van Hook discloses a coprocessor that includes a signal processor, a display processor and multiple interface units for communicating with components external to

the coprocessor. One such interface unit is the CPU interface, which facilitates the transmission of data and memory addresses between the coprocessor and the CPU (see Van Hook at Figure 5 and Figure 38). In the Final Office Action, the Examiner fails to equate any element in Van Hook to any of the elements recited in claim 1. In fact, the Examiner only states that Van Hook fails to disclose a PCE receiving commands from the CPU and controlling communication of physics data from the PPU to the host; an external memory and an internal memory; and a DME controlling the movement of data between the external memory and the internal memory in response to instructions received from the PCE. See Final Office Action at page 3. Consequently, the Examiner relies on Suzuoki to teach or suggest each and every limitation recited in previously presented claim 1.

Suzuoki discloses a computer architecture and programming model for high speed processing over broadband networks. The architecture employs a modular structure, the main module including a control processor, a plurality of processing units, a plurality of local memories from which the processing unit processes programs, a direct memory access controller, and a shared main memory. This generic architecture fails to teach or suggest the claimed PPU for several reasons.

First, in the Final Office Action, the Examiner fails completely to equate the claimed FPE to any element disclosed in Suzuoki.

Second, the Examiner appears to equate the claimed vector processor (which is included in the FPE) to the disclosed processor elements (elements 303, 305, and 307). See Suzuoki at col. 8, lines 5-23; Figure 3. However, the disclosed processing elements are not equivalent to the claimed vector processor.

The disclosed processor elements include a processing unit, a direct memory access controller (DMAC), and a plurality of attached processing units (APUs). Claim 1 makes clear that the vector processor is adapted to perform multiple, parallel floating point operations to generate physics data, the operations specified by a very long instruction word that is issued to the FPE. By contrast, the processing elements disclosed in Suzuoki are not adapted to perform multiple, parallel floating point operations to generate physics data, the operations specified by a very long instruction word (VLIW) that is issued to the FPE, as expressly claimed. More

specifically, Suzuoki discloses that each APU includes four floating point units and that the APUs are preferably SIMD (single instruction multiple data) processors. Architecturally, SIMD processors implement data level parallelism (one instruction operating on multiple sets of data) whereas VLIW processors implement instruction level parallelism (multiple instructions operating on multiple sets of data). No one skilled in the art would ever confuse these two different constructs, and Suzuoki does not teach or suggest that the operations of the floating point units may be specified in a VLIW issued to the APU.

Third, the Examiner fails to equate the claimed PCE to any element disclosed in Suzuoki. See Final Office Action at page 3. In the Final Office Action, the Examiner generally states, without any specificity, that Suzuoki discloses the PCE. In so doing, the Examiner fails to point to a single element disclosed in Suzuoki that is analogous to the PCE. In fact, the Examiner is completely silent about anything in Suzuoki that could be considered equivalent to the PCE. For this reason, and based on Applicants' review of Suzuoki, Applicants contend that Suzuoki fails to teach or suggest a PCE configured to control the overall operation of the PPU by allocating memory resources within an internal memory to the FPE and distributing commands received from a host central processing unit (CPU) to the FPE for processing, as expressly recited in claim 1.

Finally, the Examiner has attempted to equate the claimed DME with the I/O controller (element 810) and/or a bank control of the DRAM (element 1206). See Final Office Action at page 3. Again, the Examiner is not clear on what element(s) disclosed in Suzuoki is equivalent to the claimed DME. Neither the generic, conventional I/O controller nor the bank control of the DRAM is configured to control the movement of data between an external memory and the internal memory in response to instructions received from the PCE, as required by the plain language of claim 1. As discussed above, the Examiner has failed to identify any element in Suzuoki that is equivalent to the claimed PCE. Furthermore, the I/O controller, as shown and described in Figure 8 of Suzuoki, provides an interface between the chip package and the network. Suzuoki is silent as to the configuration of the I/O controller and does not describe any element that sends instructions to the I/O controller that

may be equated to the claimed PCE. Similarly, the bank controls of the DRAM are coupled to the processor element via the DMAC. The bank controls allow the PU and APUs of the processor element via the DMAC to write to a specific memory bank in the DRAM. The DMAC is controlled by the APUs and the PU in the processor element. Again, Suzuoki is silent regarding the specific configuration of the bank controls. As shown in the Figures, the bank controls are an element of the DRAM and are coupled to the processor element, neither of which the Examiner has equated to the claimed PCE. For these reasons, Suzuoki cannot and does not teach or suggest a data movement engine (DME) configured to control the movement of data between the external memory and the internal memory in response to instructions received from the PCE, as recited in claim 1.

The Examiner relies on Intel to teach a PCI or PCI-Express interface. A review of Intel shows that it has no teachings relevant to the elements and limitations of claim 1, discussed above. For these reasons, Intel fails to cure the deficiencies of Van Hook and Suzuoki set forth above.

As the foregoing illustrates, the Examiner's analysis of claim 1 is deficient in multiple ways. Consequently, no combination of the cited references teaches or suggests each and every limitation of claim 1. Therefore, these references cannot render obvious claim 1 or claims 4-8, dependent thereon. For this reason, Applicants submit that claims 1 and 4-8 are in condition for allowance. In addition, claim 9 recites limitations similar to those discussed above in conjunction with claim 1. Therefore, claim 9 is allowable for at least the same reasons as allowable claim 1. Further, claims 10-12 and 16-28 depend on claim 9 and are also in condition for allowance.

CONCLUSION

Based on the above remarks, Applicants believe that he has overcome all of the objections and rejections set forth in the Office Action mailed June 23, 2010 and that the pending claims are in condition for allowance. If the Examiner has any questions, please contact the Applicants' undersigned representative at the number provided below.

Respectfully submitted,

John C. Carey
Registration No. 51,530
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicants